



STE70NM50

N-CHANNEL 500V - 0.045Ω - 70A ISOTOP Zener-Protected MDmesh™ Power MOSFET

TARGET DATA

TYPE	V _{DSS}	R _{DS(on)}	I _D
STE70NM50	500V	< 0.05Ω	60 A

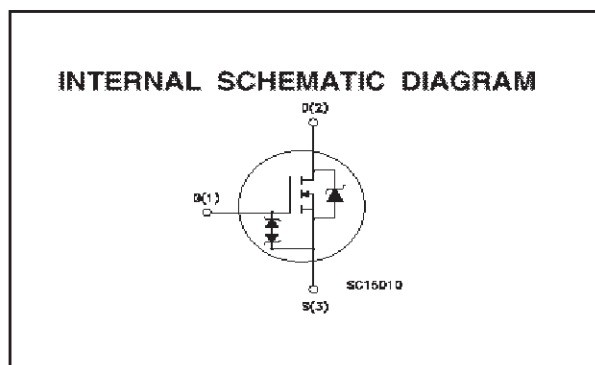
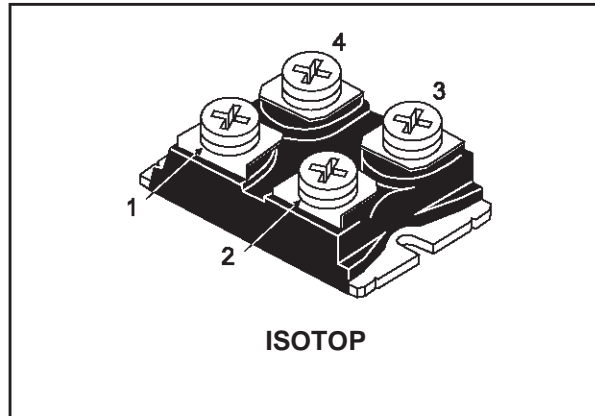
- TYPICAL R_{DS(on)} = 0.045Ω
- HIGH dv/dt AND AVALANCHE CAPABILITIES
- 100% AVALANCHE TESTED
- LOW INPUT CAPACITANCE AND GATE CHARGE
- LOW GATE INPUT RESISTANCE
- TIGHT PROCESS CONTROL
- INDUSTRY'S LOWEST ON-RESISTANCE

DESCRIPTION

The MDmesh™ is a new revolutionary MOSFET technology that associates the Multiple Drain process with the Company's PowerMESH™ horizontal layout. The resulting product has an outstanding low on-resistance, impressively high dv/dt and excellent avalanche characteristics. The adoption of the Company's proprietary strip technique yields overall dynamic performance that is significantly better than that of similar competition's products.

APPLICATIONS

The MDmesh™ family is very suitable for increasing power density of high voltage converters allowing system miniaturization and higher efficiencies.



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source Voltage (V _{GS} = 0)	500	V
V _{DGR}	Drain-gate Voltage (R _{GS} = 20 kΩ)	500	V
V _{GS}	Gate- source Voltage	±30	V
I _D	Drain Current (continuous) at T _C = 25°C	70	A
I _D	Drain Current (continuous) at T _C = 100°C	43.7	A
I _{DM} (●)	Drain Current (pulsed)	280	A
P _{TOT}	Total Dissipation at T _C = 25°C	460	W
V _{ESD(G-S)}	Gate source ESD(HBM-C=100pF, R=15KΩ)	4	KV
	Derating Factor	3.98	W/°C
dv/dt	Peak Diode Recovery voltage slope	6	V/ns
T _{stg}	Storage Temperature	-65 to 150	°C
T _j	Max. Operating Junction Temperature	150	°C

(●)Pulse width limited by safe operating area

April 2001

1/6

STE70NM50

THERMAL DATA

Rthj-case	Thermal Resistance Junction-case	Max	0.277	°C/W
Rthj-amb	Thermal Resistance Junction-ambient	Max	30	°C/W
Rthc-sink	Thermal Resistance Case-sink	Typ	0.1	°C/W
T _l	Maximum Lead Temperature For Soldering Purpose		300	°C

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I _{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T _j max)	70	A
E _{AS}	Single Pulse Avalanche Energy (starting T _j = 25 °C, I _D = I _{AR} , V _{DD} = 35 V)	TBD	mJ

ELECTRICAL CHARACTERISTICS (TCASE = 25 °C UNLESS OTHERWISE SPECIFIED)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source Breakdown Voltage	I _D = 250 μA, V _{GS} = 0	500			V
I _{DSS}	Zero Gate Voltage Drain Current (V _{GS} = 0)	V _{DS} = Max Rating V _{DS} = Max Rating, T _C = 125 °C			10 100	μA μA
I _{GSS}	Gate-body Leakage Current (V _{DS} = 0)	V _{GS} = ±30V			±100	nA

ON (1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250μA	3	4	5	V
R _{DS(on)}	Static Drain-source On Resistance	V _{GS} = 10V, I _D = 35A		0.045	0.05	Ω
I _{D(on)}	On State Drain Current	V _{DS} > I _{D(on)} × R _{DS(on)max} , V _{GS} = 10V	70			A

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g _{fs} (1)	Forward Transconductance	V _{DS} > I _{D(on)} × R _{DS(on)max} , I _D = 35A		20		S
C _{iss}	Input Capacitance	V _{DS} = 25V, f = 1 MHz, V _{GS} = 0		7500		pF
C _{oss}	Output Capacitance			980		pF
C _{rss}	Reverse Transfer Capacitance			200		pF
R _G	Gate Input Resistance	f=1 MHz Gate DC Bias = 0 Test Signal Level = 20mV Open Drain		1.5		Ω

Note: 1. Pulsed: Pulse duration = 300 μs, duty cycle 1.5 %.

ELECTRICAL CHARACTERISTICS (CONTINUED)
SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	$V_{DD} = 250V, I_D = 35A$		TBD		ns
t_r	Rise Time	$R_G = 4.7\Omega, V_{GS} = 10V$ (see test circuit, Figure 3)		TBD		ns
Q_g	Total Gate Charge	$V_{DD} = 400V, I_D = 70A,$ $V_{GS} = 10V$		240	336	nC
Q_{gs}	Gate-Source Charge			TBD		nC
Q_{gd}	Gate-Drain Charge			TBD		nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{r(Voff)}$	Off-voltage Rise Time	$V_{DD} = 400V, I_D = 70A,$		TBD		ns
t_f	Fall Time	$R_G = 4.7\Omega, V_{GS} = 10V$ (see test circuit, Figure 5)		TBD		ns
t_c	Cross-over Time			TBD		ns

SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				70	A
$I_{SDM(2)}$	Source-drain Current (pulsed)				280	A
$V_{SD(1)}$	Forward On Voltage	$I_{SD} = 70A, V_{GS} = 0$			1.5	V
t_{rr}	Reverse Recovery Time	$I_{SD} = 70A, di/dt = 100A/\mu s,$ $V_{DD} = 60V, T_j = 150^\circ C$ (see test circuit, Figure 5)		TBD		ns
Q_{rr}	Reverse Recovery Charge			TBD		μC
I_{RRM}	Reverse Recovery Current			TBD		A

Note: 1. Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.
 2. Pulse width limited by safe operating area.

Fig. 1: Unclamped Inductive Load Test Circuit

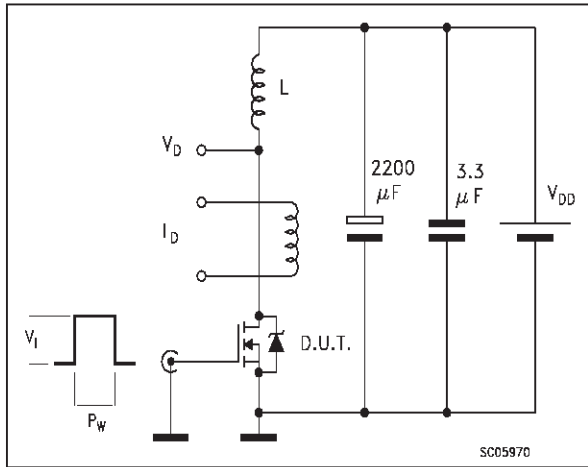


Fig. 2: Unclamped Inductive Waveform

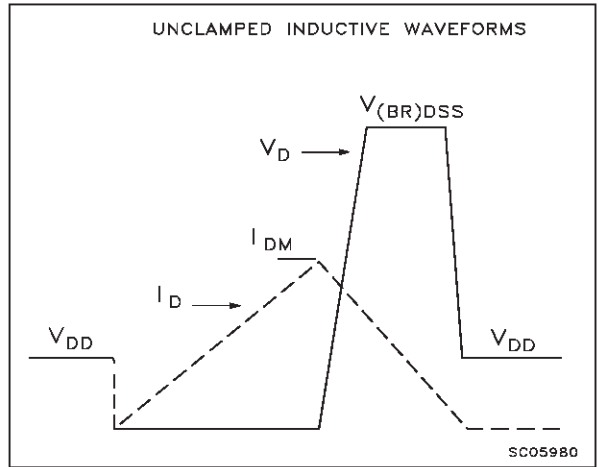


Fig. 3: Switching Times Test Circuit For Resistive Load

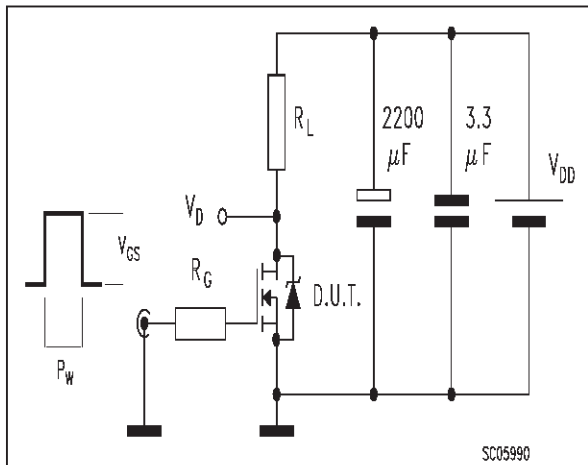


Fig. 4: Gate Charge test Circuit

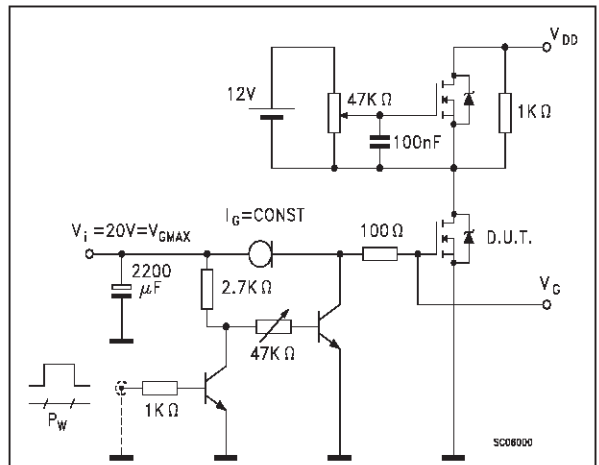
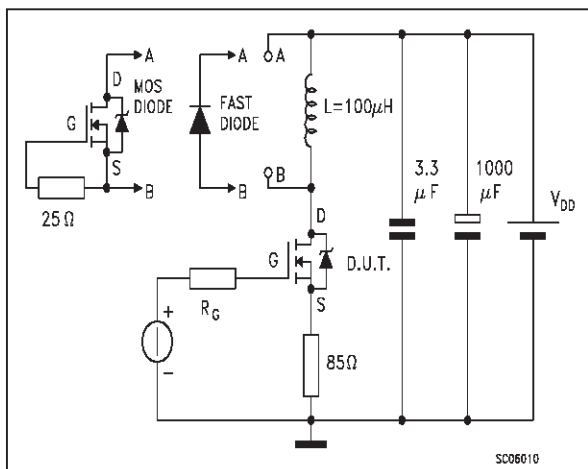
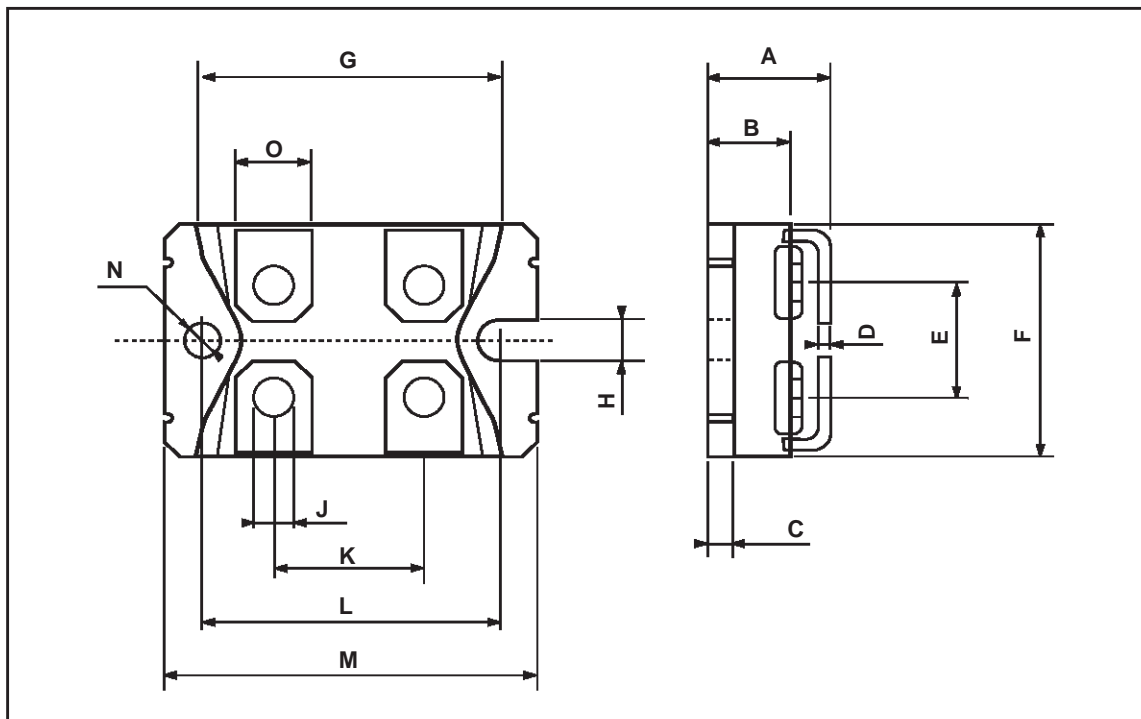


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



ISOTOP MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	11.8		12.2	0.466		0.480
B	8.9		9.1	0.350		0.358
C	1.95		2.05	0.076		0.080
D	0.75		0.85	0.029		0.033
E	12.6		12.8	0.496		0.503
F	25.15		25.5	0.990		1.003
G	31.5		31.7	1.240		1.248
H	4			0.157		
J	4.1		4.3	0.161		0.169
K	14.9		15.1	0.586		0.594
L	30.1		30.3	1.185		1.193
M	37.8		38.2	1.488		1.503
N	4			0.157		
O	7.8		8.2	0.307		0.322



Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specification mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

The ST logo is a trademark of STMicroelectronics

© 2000 STMicroelectronics – Printed in Italy – All Rights Reserved

STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - China - Finland - France - Germany - Hong Kong - India - Italy - Japan - Malaysia - Malta - Morocco -
Singapore - Spain - Sweden - Switzerland - United Kingdom - U.S.A.

<http://www.st.com>